High Power High Efficiency Class-J GaN HEMT Amplifier with Non-Foster Network

Charles Nwakanma Akwuruoha[1], Agwu Ogbonnaya Ekwe[2] and Zhirun Hu[3]
[1,2]Department of Electrical/Electronic Engineering, Michael Okpara University of Agriculture Umudike, Nigeria.
[3]School of Electrical and Electronic Engineering, The University of Manchester, United Kingdom.
[1]akwuruoha.charles@mouau.edu.ng, [2]ogbonnaekwe@gmail.com and [3]Z.Hu@manchester.ac.uk

ABSTRACT
This paper proposes high power high efficiency Class-J GaN HEMT amplifier with non-Foster network. Non-Foster network forms part of the input matching network of the power amplifier (PA) and cancels out the power transistor input parasitic capacitance thereby enhancing output power, power added efficiency, drain efficiency and transducer power gain. The PA design was based on Cree's CGHV40030FP GaN HEMT biased with drain supply voltage of 50 V at quiescent drain-to-source current (I_{DSq}) of 15 mA. The two GaN HEMTs in the non-Foster network were each biased with drain supply voltage of 20 V at IDSq of 3 mA. The PA operates from 2.0 to 2.2 GHz. The non-Foster negative capacitance at 2.1GHz center frequency stood at -2.4 pF. The power amplifier has output power of 43.9 dBm (24.5 W), 69.3% drain efficiency, 66.4% power added efficiency (PAE) and transducer power gain of 11.9 dB.

Keywords: Class-J, GaN HEMT, Negative Capacitance, Non-Foster Network, Power Amplifier, Power Transistor

I.0 INTRODUCTION

Non-Foster networks are used in microwave circuits to generate the negative capacitance or inductance required to cancel out power transistor parasitic capacitance to enhance performance. In the work proposed in this paper, non-Foster network have been used to enhance PA output power, efficiency and gain. This paper reviews the work proposed in [1]. The non-Foster networks violate Foster reactance theorem. Non-Foster networks have positive reactance-frequency slope and reflection coefficient which move in clockwise direction with respect to frequency on Smith chart. Non-Foster networks hereafter referred to as non-Foster circuits (NFC) are classified into negative impedance converters (NIC) and negative impedance inverters (NII) [2]-[4]. The NIC generates the negative capacitance which cancels out the input parasitic capacitance of the power transistor. Linvill [5] first proposed the use of active circuits to implement NIC whereby the NIC was described as four-pole network with input current equal to output current. The NIC hereafter referred to as NFC can be classified as open circuit stable or short circuit stable and has an input voltage equal to the negative of the output voltage [5]. NFC have been used to enhance the bandwidth of antennas [2], [4]-[6]. NFC have reportedly been used in Doherty power amplifier (DPA) to enhance the bandwidth [7]. In [8] NFC was also used to enhance the gain of CMOS distributed amplifier (DA). NFC have been reportedly used in [9] as inter-stage matching network of GaN pHEMT PA.

In this work, detailed stability analysis have been carried out to forestall oscillations which could hamper the effective performance of the PA in terms of output power, power added efficiency, drain efficiency and transducer power gain. The combination of Class-J topology and NFC mitigates the effects of transistor input/output parasitic capacitance. This paper is structured as follows. Class-J theory is discussed in section II. Section III treats NFC theory and design. In section IV, the proposed PA circuit design and results are discussed. Section V concludes the paper.

2.0 CLASS-J THEORY

Class-J power amplifier aims to mitigate the effect of transistor drain-to-source capacitance on the fundamental load of the PA by the application of reactive termination to the fundamental to changing it from resistive to reactive regime [10]-[13]. In Class-J mode, higher order even harmonics than the second harmonic do not exist as the third harmonic is considered short. The output voltage and output current are 45° out of phase. The fundamental and second harmonic components of impedances respectively denoted by Z_O and Z_S are related to the load resistance (R_L) by

$$Z_O = R_L + jR_L \quad (1)$$

$$Z_S = -j3\pi/8R_L \quad (2)$$

3.0 NFC THEORY AND DESIGN

A. Theory

The relationship between reactance (X) and susceptance (B) with angular frequency (ω) of Foster and non-Foster circuits respectively denoted by X_{FC} and X_{NFC} are given by (4) and (5) [3] whereby the derivatives of the reactance and susceptance with angular frequency is greater than zero for Foster circuit and less than zero for non-Foster circuit.

$$dX_{FC} / d\omega > 0 \text{ and } dB_{FC} / d\omega > 0 \quad (4)$$

$$dX_{NFC} / d\omega < 0 \text{ and } dB_{NFC} / d\omega < 0 \quad (5)$$

B. Non-Foster Circuit Design

The non-Foster schematic circuit is shown in Fig. 1. The NFC was designed based on Cree CGHV40030FP packaged transistor. The transistor was biased with drain supply voltage of 20 V at quiescent drain-to-source current of 3 mA. The DC I-V characteristics bias points of the GaN HEMTs in the NFC and PA are shown in Fig. 2. The NFC consists mainly of microstrip transmission lines, inductors and capacitors. The microstrip lines have dielectric constant of 4.6 and thickness of 1.6mm. The dimension of the transmission lines (in mm) are shown as width/length. The NFC input impedance characteristics showing the magnitude and imaginary part of input impedance indicates a negative reactance to frequency slope across the 200 MHz bandwidth are shown in Fig. 3. The NFC effective negative capacitance from 2.0 to 2.2 GHz is shown in Fig, 4. The NFC effective negative capacitance from 2.0 to 2.2 GHz stood at -1.9 to -6.9 pF.

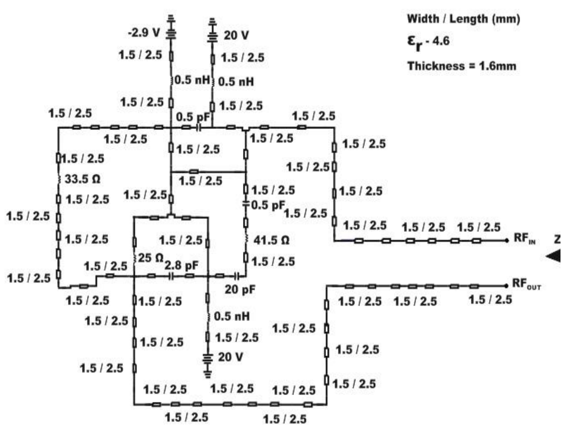

Fig. 1: NFC Schematic Circuit

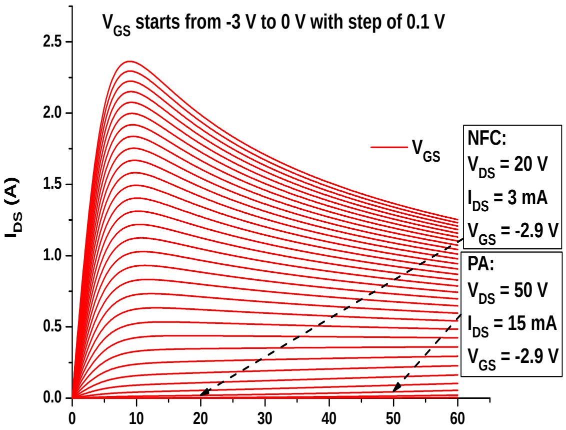

Fig. 2: NFC and PA Bias Points

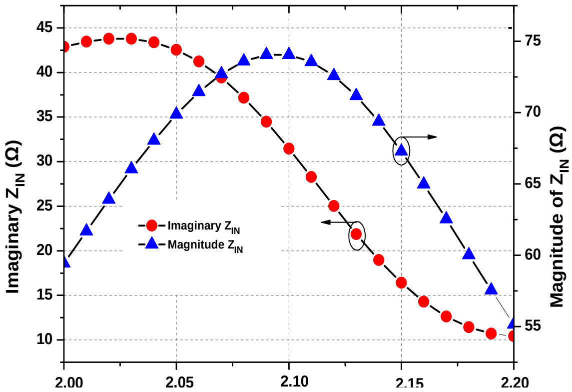

Fig. 3: Magnitude and Imaginary Part of Input Impedance

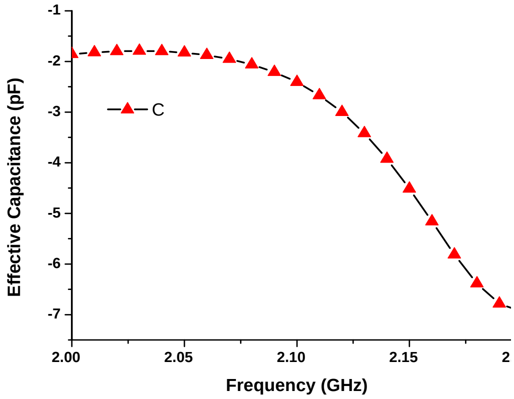

Fig. 4: Effective Capacitance

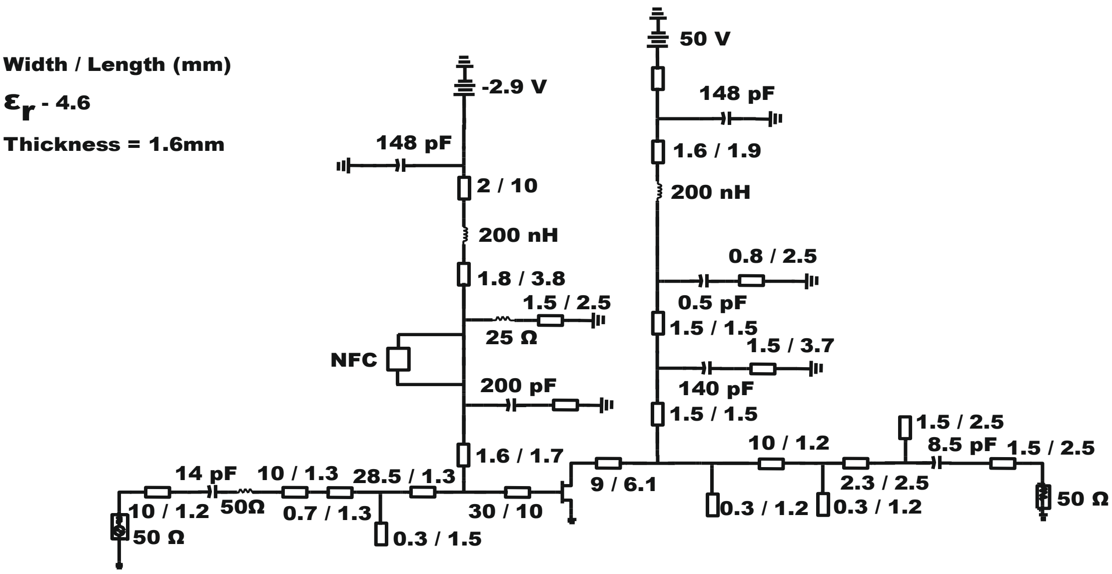

Fig. 5: The PA Schematic Circuit Diagram

4.0 PA CIRCUIT DESIGN AND RESULTS

A. PA circuit design

The PA schematic circuit is shown in Fig. 5. The PA was designed based on Cree's packaged GaN HEMT (CGHV40030FP) biased with drain supply voltage of 50V at quiescent drain-to-source current of 15 mA as shown in the bias points in Fig. 1. Source and Load pull simulations were used to obtain the respective source and load impedances required to synthesize the input and output matching networks to achieve maximum output power. The NFC was stabilized, simulated and confirmed to be unconditionally stable prior to the introduction into the input matching network of the power amplifier. The NFC forms part of the input network of the PA. The main components of the PA are microstrip transmission lines with dielectric constant of 4.6 and thickness of 1.6mm, capacitors, resistors and inductors. The transmission lines width/length (mm) are shown in the schematic. The PA was terminated with source and load impedance of 50Ω.

B. Results

The results will be discussed in accordance with small signal stability result and large signal harmonic balance simulation result.

(a) *Small Signal Simulation*

Small signal S-parameter simulation was carried out to determine the stability of the PA. The PA was found to be unconditionally stable as shown in Fig. 6. The stability considerations in this work are two-fold: the Rollet stability factor/measure [14] and Nyquist stability criterion. The stability factor and measure are greater than unity and positive, respectively. The Nyquist stability criterion shown in Fig. 7, indicates unconditional stability as the input return loss did not encircle the origin [15].

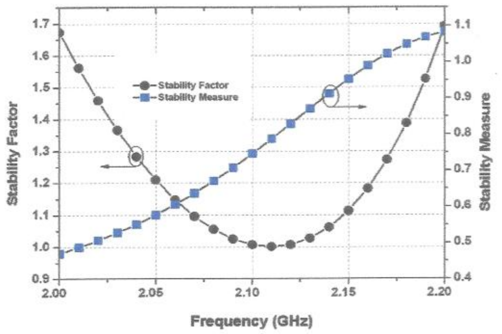

Fig. 6: Stability Factor and Stability Measure

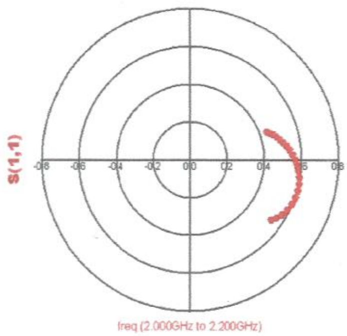

Fig. 7: Nyquist Stability Criterion

4.1 Large Signal Simulation

One-tone harmonic balance simulation was carried out on the PA in two instances. In the first instance, the input power was swept from 0 to 32 dBm at 2.1 GHz center frequency and the results are shown in Figs. 8 and 9. The result indicates that the PA has 69.8% drain efficiency, 66.75% PAE, 43.9 dBm (24.5 W) output power and transducer power gain of 11.9 dB. In the second instance, the frequency was swept from 2.0 to 2.2 GHz at input power of 32 dBm. The result is shown in Fig. 9 wherein between 2.0 to 2.2 GHz frequency range, the PA has the following range of results. 68.7 to 60.3% drain efficiency, 66.1 to 55.5% PAE, 44.6 to 43.9 dBm of output power, and 12.6 to 10.3 dB transducer power gain. A comparison of the PA performance with other reported NFC PAs, indicates that the PA compares well with the reported state-of-the-art values as shown in Table. I.

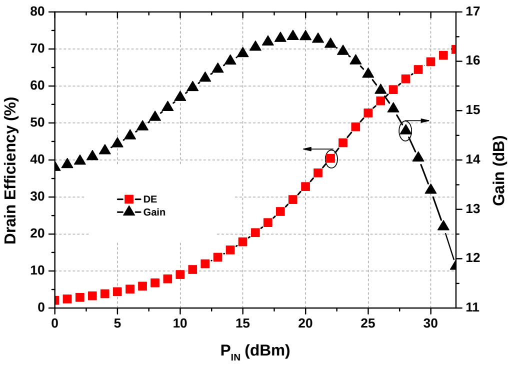

Fig. 8: Drain Efficiency (DE) and Gain versus Input Power

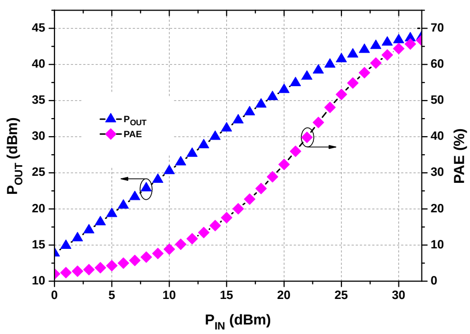

Fig. 9: Output Power and PAE versus input

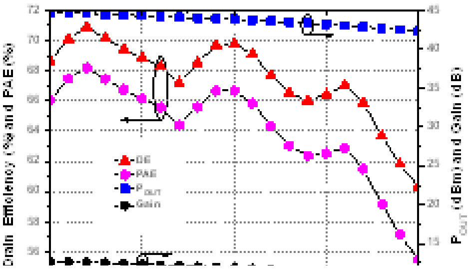

Fig. 10: Drain Efficiency (DE), Output Power, PAE and Gain versus Frequency

TABLE I: PA State-of-the Art Values

Ref.	Topology	Frequency (GHz)	PAE (%)	Pout dBm	Gain (dB)
[8]	DPA	1.9-2.2	68	30	-
[9]	DA	0-32	-	21.3	13.2
[10]	NMPA	6-18	21	37.5	19.1
[This Work]	Class-J	2.0-2.2	66.7	43.9	11.9

CONCLUSION

A high power high efficiency class-J GaN HEMT amplifier with non-Foster network has been proposed, designed and simulated. The simulation results indicate that good transducer power gain, high efficiency and high output power can be achieved if a non-Foster matched Class-J PA is made unconditionally stable across the operational bandwidth. The proposed PA will find suitable applications in microwave circuits/devices where there is desirability for high power and high efficiency.

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